

AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A method of ~~manufacturing~~ monitoring a reduction in thickness of a bonded pair of semiconductor wafers, having an first active wafer and a second wafer (1,2), by monitoring a reduction in thickness of one of the wafers during manufacturing, the method comprising

- forming a test structure having a systematic row of trenches in ~~an~~ the active wafer, said trenches having different defined widths, said active wafer provided for receiving an active circuit in a later step;
- bonding the active wafer with a side which holds the test structure onto the second wafer of the semiconductor wafer pair;
- wherein a targeted thickness of the active wafer ~~after~~ during a removal of wafer material corresponds at least substantially to a reference depth of a reference trench in the row of trenches in said test structure, said reference trench neighboured by a shallower and a deeper trench;
- performing the wafer material removal ~~process comprising a polishing process,~~ commencing from a backside of the bonded active wafer until the reference trench is exposed, and optically detecting said exposure of the reference trench, ~~detected~~ for monitoring a thickness reduction of the active wafer; and
- forming at least one ~~an~~ active circuit in said active wafer in said later step.

2. (Currently Amended) The method of claim 1, wherein the systematic row comprises trenches of different, increasing depths, and the material removal comprises a polishing step.

3. (Previously Presented) The method of claim 2, wherein deep trenches are formed in an etch process using an etch mask having openings of different widths for the trenches of different widths.

4. (Previously Presented) The method of claim 1, wherein the trenches are not filled or unfilled prior to bonding the active wafer to the second wafer.
5. (Previously Presented) The method of claim 1, wherein the active wafer is a wafer formed of a semiconductor crystal.
6. (Previously Presented) The method of claim 1, wherein the second wafer at least comprises an insulating layer.
7. (Previously Presented) The method of claim 1, wherein the systematic row is a sequence of trenches that become continuously shallower or continuously deeper.
8. (Previously Presented) The method of claim 1 or 7, wherein the trenches are formed as stripe-like trenches each having a certain depth and width, and wherein a respective depth increases as the corresponding width increases.
9. (Currently Amended) The method of claim 1, wherein prior to reaching a bottom of the reference trench by the removal process, and prior to exposing the reference trench, the removal process is interrupted at least once for one of an optical monitoring and observation, as said optical detection.
10. (Currently Amended) A device for monitoring a reduction in thickness of a bonded semiconductor wafer pair comprised of a first and a second wafer, the device comprising
 - a test structure of a systematic row of a plurality of trenches, each having a different width ~~widths~~ in a defined manner and formed in the first wafer, said first wafer comprising an active circuit, wherein
 - said active wafer ~~is bonded with a side, in which the test structure is provided or was formed~~, onto the second wafer of the semiconductor wafer pair;

- a thickness of the active wafer substantially corresponds to a depth of a reference trench of the test structure as a ~~target~~targeted thickness during a removal process from ~~a the~~ backside of the active wafer when ~~until~~ the reference trench is exposed and the bottom thereof is removed by the removal process~~of the reference trench was exposed~~.

11. (Previously Presented) The device of claim 10, wherein the trenches are not filled with a fill material.

12. (Previously Presented) The device of claim 10, wherein systematic row of trenches of different depths comprises a systematic configuration with respect to the widths of the trenches such that the trenches are broader the more deeply they are formed in the first as active wafer.

13. (Previously Presented) The method of claim 1, wherein the targeted thickness is the desired or a predefined target thickness.

14. (Currently Amended) The method of claim 9 or 1, wherein an optical device is directed towards the backside of the active wafer for the optical detection, and the removal process comprising at the polishing process, ~~is performed from the backside and terminating~~is terminated when the an optical detection~~observation~~ reveals exposure of a bottom end of the reference trench, ~~an optical device is directed towards the backside of the active wafer fore such optical observation.~~

15. (Previously Presented) The device of claim 10, wherein the reference trench is located in a central region of the systematic row and on one side of the reference trench at least one or more trenches of smaller depth are located, and at the other side of the reference trench one or more trenches of greater depth are located.

16. (Previously Presented) The device of claim 15, wherein on one side at least one or more trenches of smaller width and on the other side at least one or more trenches of greater width are located.

17. (Previously Presented) The method of claim 1, wherein the second wafer is a carrier wafer.

18. (Previously Presented) The method of claim 1, wherein the row of trenches comprising a plurality of parallel trenches, each having a different width.

19. (Previously Presented) The method of claim 1, wherein the neighbouring trenches are several deeper and several shallower trenches.

20. (Currently Amended) The method—~~Method~~ of claim 3, wherein the etch process is performed ~~in particular~~ prior to bonding the active wafer onto the second wafer as carrier wafer.

21. (Currently Amended) The method—~~Method~~ of claim 4, the not filled trenches being open prior to said bonding.

22. (Currently Amended) The method—~~Method~~ of claim 5, the active wafer is comprised of silicon.

23. (Currently Amended) The method—~~Method~~ of claim 6, the second wafer as carrier wafer comprises the insulating layer formed of silicon dioxide.

24. (Currently Amended) A method of monitoring a reduction in thickness during a production of a bonded pair of semiconductor wafers, having an active and a carrier ~~first and a second~~ wafer; ~~(1,2);~~
the method comprising:

forming a test structure having a systematic row of trenches in ~~said~~a active wafer, said trenches having different defined widths, said active wafer provided for receiving an active circuit in a later step;

bonding the active wafer with a side which holds the test structure onto the ~~carrier~~second wafer of the ~~pair of semiconductor wafers;~~wafer pair;

performing ~~a~~the wafer material removal ~~process~~ comprising a polishing process, commencing from a backside of the bonded active wafer until ~~a~~the reference trench is exposed, and optically ~~detecting the exposed~~detected for monitoring ~~a~~ thickness reduction of the active wafer down to a target thickness; and

forming an active circuit in said active wafer in said later step;

wherein ~~the target~~a targeted thickness of the active wafer upon said material ~~during a~~ removal corresponds to a depth of ~~said~~a reference trench of the row of trenches in said test structure, said reference trench neighbored by a shallower and a deeper trench, and said ;

~~wherein the~~ neighbouring trenches are several deeper trenches on one side of the reference trench and several shallower trenches on the other side of the reference trench.